ADVANCED 6/4 GHz RECEIVER FOR SPACE APPLICATION

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ABSTRACT

This paper describes an advanced 6/4 GHz satellite receiver developed in order to meet the extended WARC 79 frequency allocation needs. The receiver provides low-noise and very low level of in-band spurious signals over an extended 750 MHz bandwidth. This highly reliable receiver utilizes the state of the art packaged FET space qualified at the present time and meets very stringent requirements over a qualification temperature range of -5 to + 55°C. Details of the design and measured performance is given.

INTRODUCTION

SPAR has been designing and building communication satellite receiver since early 1970's, however due to the extended WARC 79 frequency allocations, a new family of receivers had to be developed in order to cover the future needs in the WARC 79 frequency plan.

The uplink frequency band (5.75 - 6.5 GHz) the receiver was tuned falls within the region 1** of the WARC 79 uplink frequency allocation, but the receiver front end was designed to cover 1 GHz of the uplink frequency bandwidth. The uplink frequencies are down converted to 3.45 to 4.2 GHz covering therefore almost the entire WARC 79 down link subband. (800 MHz B.W.)

Details of the electrical and mechanical structure of this light weight, easily reconfigurable receiver designed to operate over a wide temperature range is presented.

All components used in the receiver are space qualified, the test results of an integrated breadboard unit that was manufactured and assembled using flight approved processes is presented.

The receiver reconfigurability is achieved by using a modular approach, therefore changes in receiver gain can be met by changing attenuator settings in the RF slice or by substituting amplifier stages by section of 50 OHM lines, changes in frequency plan are accomodated by retuning the RF slice and replacing input and local oscillator filters.

RECEIVER DESCRIPTION

The receiver consists of four principal components: the input waveguide bandpass filter; the microwave (rf) slice; the local oscillator (LO) slice; the waveguide evanescent bandpass filter.

An incident 6 GHz signal passes through the input bandpass filter and into the rf slice where it is amplified by a 6 GHz amplifier chain. The signal frequency is then converted from 6 GHz to 4 GHz by combining the input signal with a 2 GHz LO signal thru a single balanced diode mixer. The resulting 4 GHz signal is amplified by a 4 GHz amplifier chain before passing out of the receiver. The Local Oscillator signal is obtained by taking the output of an oven-controlled crystal oscillator and using a chain of amplifiers and frequency multipliers to obtain the correct signal amplitude and frequency. Regulated voltage supplies for the active modules are derived from an electronic power conditioner (EPC) which operates directly from the space-craft bus.

The LO slice and rf slice are contained in separate housings which are bolted back-to-back to form a single module. This arrangement gives a compact unit with good electrical isolation between the slices whilst giving extra flexibility in that it allows the rf and LO slices to be marketed separately, it allows the rf slice to be used with different LO slices and vice versa (subject to mechanical compatibility) and allows one LO slice to be used for several rf slices.

The EPC is contained within the LO slice housing and the rails necessary for the rf slice active module biases pass

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between the two slices in a shielded channel. The shielded channel i necessary to ensure that the required rf susceptibility ratio is achieved. A gasket is included on both the LO and the rf slice housing between the respective chassis covers and bodies. These gaskets are also for rf protection.

LOCAL OSCILLATOR DESCRIPTION

A block diagram of the Local Oscillator is given in Figure 1.0. The signal source is a 109.5 MHz Colpitts-type crystal oscillator in which the crystal is installed in a temperature controlled oven to minimize frequency variations due to changes in temperature of the receiver operating environment. The crystal oscillator is followed by a broad-band buffer which ensures that the oscillator operates into a 50 ohm load. A bipolar tripler is used to multiply the carrier frequency to 328.6 MHz. The signal is then filtered and amplified by a bipolar class-B amplifier to the level necessary for correct operation of the step-recover diode X7 multiplier. At the output of the SRD multiplier is an isolator which is necessary to correctly load the SRD output and thus prevent parametric oscillations. Following the isolator is an MIC bandpass filter which removes unwanted signals at $\pm$328 MHz from the carrier.

The output level from the local oscillator is controlled by a ALC loop. A PIN attenuator is used to set the signal level, the attenuation level being determined by sampling the rf signal using a coupler/detector and comparing the detector output with a reference voltage developed in the ALC comparator.

Spurious signals are removed from the local oscillator output by use of an evanescent mode waveguide bandpass filter and a low pass filter. The low-pass filter is necessary to remove high frequency spurious responses which would not be eliminated by the evanescent mode filter.

INPUT WAVEGUIDE BANDPASS FILTER DESCRIPTION

The input filter is an 11-pole Chebyshev filter with a 0.01 dB ripple factor. It is a direct-coupled filter which has been realized using inductive posts in a rectangular waveguide (WR159). The filter has a high unloaded Q which results in a low insertion loss.

ELECTRONIC POWER CONDITIONER (EPC) DESCRIPTION

The EPC is a push-pull, pulse width modulated (PWM) converter which operates at 200 kHz. This configuration is chosen because it gives the most efficient use of the power transformer and it yields a minimum size of input and output filters because of the frequency doubling effect.

The PWM system gives approximately constant efficiency for all output levels and yields a high degree of flexibility in that the EPC is able to operate over a wide range of input voltages and output power levels. A block diagram of the EPC is given in Figure 2.0.

The PWM controller and protection circuit are the heart of the power supply. THe control circuits drives the switching transistors directly. HEXFET's have been chosen for the switching transistors to achieve optimum drive current levels, power gain and switching speed together with a high degree of stability of power gain and switching speed against temperature variations.

The output from the power transistors is transformed to the required secondary voltage and then rectified by fast switching diodes. Output LC filters are included on each rail to achieve the required ripple levels and to assure the proper output impedance characteristics. A feedback loop is icluded at the output to achieve a regulation of better than 2%.

Other features of the EPC are an auxilliary power supply to provide the voltage and current to the control circuit prior to turn-on of the unit, and under-voltage, over-voltage and over-current protection circuits.

RF SLICE DESCRIPTION

A block diagram of the rf slice, is shown in Figure 3.0. A waveguide to MIC transition, which is an integral part of the rf slice chassis, is used to transfer the 6 GHz input signal from a waveguide mode to a microstrip mode suitable for processing by solid-state MIC components.

The 6 GHz signal is amplified by a broadband (1.0 GHz B.W.) two-stage low noise FET amplifier before being down-converted to 4 GHz by combining it with the 2 GHz local oscillator signal in a single-balanced diode mixer.

The mixer is followed by a 7-pole notch filter which removes the second harmonic of the local oscillator. If this harmonic were not removed it would be amplified by the 4 GHz amplifier chain ($2xf_{LO}$ = 4.6 GHz) and saturate the

output stages.

The 4 GHz signal resulting from the mixing process is amplified to the required output level by a chain of 4 GHz amplifiers. There are three 4 GHz amplifiers: a two-stage FET interstage amplifier; a two-stage FET drive amplifier; a one-stage FET output amplifier. The interstage and driver amplifiers are identical. All these amplifiers were tuned over 800 MHz Bandwidth (3.4 - 4.2 GHz).

Included in the 4 GHz chain is a PIN diode attenuator. This attenuator is in three sections with each section performing a different function. The three sections are a variable attenuator, a fixed attenuator and a switched attenuator. The variable attenuator allows compensation of receiver gain over temperature, the fixed attenuator allows the gain of the receiver to be set to the required value at ambient temperature during receiver alignment, the switched attenuator allows compensation of receiver gain over life and also allows the gain of the receiver to be increased if the input signal level drops. The switched attenuator is the only section of the attenuator that can be controlled remotely. This unit also meets its module performance requirements over 800 MHz bandwidth.

Isolators are used at the input and output ports to minimize input and output port VSWR's. Isolators are also used between the various modules in the rf chain to minimize interaction between the modules and thus reduce gain ripple. These isolators also help to prevent changes in gain slope and gain ripple over temperature.

These MIC "drop in" type isolators exceeds its required specifications over 800 MHz bandwidth.

The amplifiers are biased from individual bias supplies which are located within the rf slice housing but in a separate compartment from the rf modules.

The only connections between the bias module and rf module compartments are dc connections which are made via filtercons to give good isolation between the two compartments and thus help reduce spurious outputs from the receiver. The bias circuits are temperature sensitive to allow the biases on the various active components to be controlled over temperature to allow compensation of the receiver response.

A photograph of the integrated receiver is given in Figure 4.0, and a summary of the test results against the target performance presented in Table 1.0.

CONCLUSION

The design and measured performance of an integrated breadboard 6/4 GHz satellite communication receiver have been presented, its measured performance indicates that this receiver offer outstanding transmission characteristics over the WARC 79/RARC 83 6/4 GHz frequency allocation.

Its high gain capability (68.0 dB), high intercept point (+31 dBm), low noise figure (2.1 dB), low group delay (3.1 nsec.) broader bandwidth (750 MHz) all achieved with low power consumption (4.6 W) combined with low weight and size, makes this receiver a very attractive alternative for future C-Band satellite transponder usage.

ACKNOWLEDGEMENTS

This work has been performed under the sponsorship of the Canadian Department of Communication Space Industry Development Program Contract No. 21ST-36100-3-0316. The authors would like to thank Mr. G. Larmour for performing the tests of the unit and Dr. M. Stubbs from the Department of Communication for useful discussions and support.

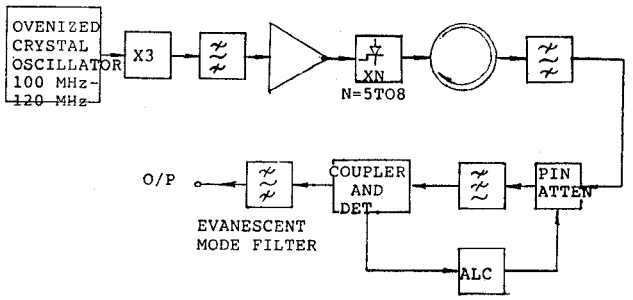

FIG. 1: L.O. SLICE BLOCK DIAGRAM

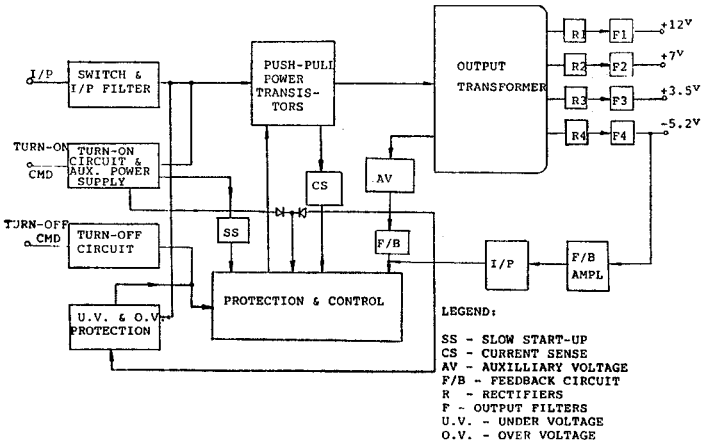

FIG .2: ELECTRONIC POWER CONDITIONER BLOCK DIAGRAM

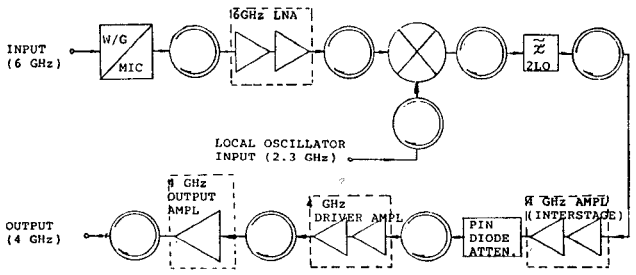

FIG. 3: RF SLICE BLOCK DIAGRAM

PARAMETER	TARGET SPECIFICATION	MEASURED PERFORMANCE	COMMENTS
(1) Input Frequency Range (GHz)	5.865 - 6.665	5.750 - 6.500	Frequencies clipped to avoid high level in-band mixer products.
(2) Output Frequency Range (GHz)	3.400 - 4.200	3.450 - 4.200	
(3) Translation Frequency (GHz)	2.465	2.300	
(4) Gain (dB) [attenuator set to 0dB] *	55 - 70	67.5	
(5) Gain Stability (dB/15°C) *	0.3	0.275	
(6) Gain Control (dB) *	4.5 ± 0.5	4.47 ± 0.2	
(7) Gain Flatness * (a) dB p-p/750MHz (b) dB p-p/36MHz	0.5 0.2	0.50 0.20	
(8) Gain Slope (dB/MHz) *	0.008	0.008	
(9) Gain Slope Change (dB/MHz) *	0.006	0.0047	
(10) Noise Figure (dB) *	3.2	2.2	Including input waveguide filter
(11) Input/Output VSWR	1.2:1	1.19:1	DC power on and off
(12) Group Delay Variation (a) Operating band; nsec/750 MHz (b) Channel BW; nsec/40 MHz	5 1	3 1	
(13) Power Consumption (W) *	6	4.6	At 28V supply
(14) Spurious Outputs (a) In-band (dBm/4 kHz) (b) Out-of-band (dBm/4 kHz) (c) LO harmonics (dBm)	-88 -35	-90 -42	2 x f_{LO}
(15) Temperature Range (°C) (a) Acceptance (b) Qualification (c) Turn-On	0 to +50 -5 to +55 -35 to +55	0 to +50 -5 to +55 -35 to +55	
(16) Out-of-band Rejection of Input Filter (dB) (a) F_O -656 MHz (b) F_O +710 MHz	20 30	44 52	
(17) Receiver Gain at 4 GHz (dB)	-15	6.5	High gain state and without I/P waveguide filter
(18) Two-Tone Third Order Intermod * (a) Intercept Point (dBm) (b) Each tone O/P level/I/P level (dBm/dBm)	+30 +10/-30	+31 +10/-32	
(19) Single Carrier Phase Shift Output Level/Phase	+16 dBm/1.5 deg	0.69	Low gain state
(20) Weight (kg)	1.6	1.841	RF and LO chassis not weight relieved

TABLE 1: SUMMARY OF INTEGRATED BREADBOARD TEST RESULTS

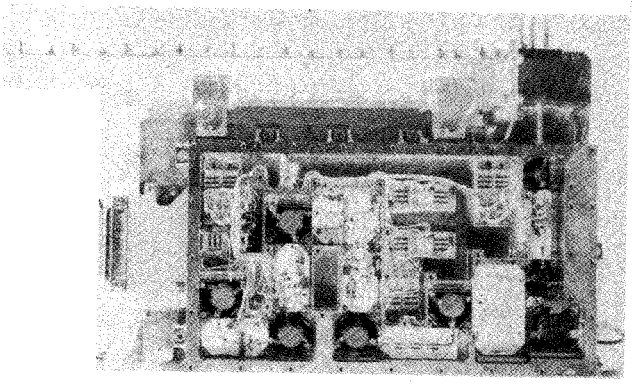

FIG. 4: INTEGRATED RECEIVER: VIEW OF RF SLICE